30V, 7.5 MHz, Low Bias Current, Single Supply, RRO, Precision Op Amp

Preliminary Technical Data

ADA4622-2

FEATURES

Next Generation of Popular AD820/2/4 Family
Wide Bandwidth: 7.5 MHz Typical
High Slew Rate: 20 V/μs Typical
Low Input Bias Current: 5 pA Maximum at 25°C
Low Offset Voltage: 1 mV Maximum at 25°C
Low Offset Voltage Drift: 2 μV/°C Typical, 10 μV/°C Maximum
Single and Dual Supply Operation
- **Input voltage range includes V-**
- **Rail-to-Rail Output**

Input EMI Filters
Industry Standard Package and Pinouts

APPLICATIONS

High Output Impedance Sensor Interface
Photodiode Sensor Interface
Transimpedance Amplifier
ADC Driver
Precision filters and signal conditioning

PIN CONFIGURATIONS

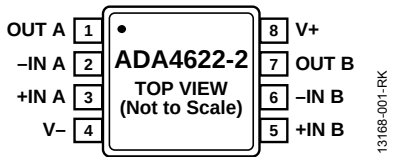

Figure 1. 8-lead, SOIC_N (R Suffix) and 8-lead, MSOP (RM Suffix) Pin Configuration

GENERAL DESCRIPTION

The ADA4622-2 is the next generation of the popular AD822 Single Supply, RRO, Precision JFET input op amp. The ADA4622-2 includes many improvements that make it desirable as an upgrade without compromising the flexibility and ease of use that made the AD822 so useful for a wide variety of uses and applications.

The input voltage range includes the minus supply and the output swings rail-to-rail. Input EMI filters have been added to increase the signal robustness in the face of closely located switching noise sources.

The speed in terms of bandwidth and slew rate have been increased along with a stronger output drive to improve settling time performance and enable it to drive the inputs of modern single-ended SAR Analog-to-Digital Converters.

Voltage noise has been reduced, both broadband by 25% and 1/f by half, while holding the supply current constant. DC Precision has been improved with half the offset and a maximum thermal drift specification has been added. The Common Mode Rejection Ratio has been improved to make it more suitable when used in non-inverting gain and difference amplifier configurations.

The ADA4622-2 is specified for operation over the extended industrial temperature range of -40 °C to +125 °C and operates from 4.5V to 30V with specifications at 5 V, ±5 V, and ±15 V. The ADA4622-2 will be in SOIC-8 and MSOP-8.

Rev. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS V_{SY} = ±15 V

V_{SY} = ±15 V, V_{CM} = V_{OUT} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.04	±0.8	mV
		-40°C < T_A < +125°C			TBD	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C < T_A < +125°C		2	10	µV/°C
Input Bias Current	I_B			2	±10	pA
		-40°C < T_A < +125°C	–TBD		+TBD	pA
		V_{CM} = V-		-15		pA
Input Offset Current	I_{OS}				±10	pA
		-40°C < T_A < +125°C	–TBD		+TBD	pA
Input Voltage Range	IVR		V- - 0.2		V+ - 1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V- to V+ - 3 V	84	100		dB
		–40°C < T_A < +125°C	TBD			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_{OUT} = –14.5 V to +14.5 V	117	122		dB
		–40°C < T_A < +125°C	TBD			
		R_L = 1 kΩ, V_{OUT} = –14 V to +14 V	102	110		dB
		–40°C < T_A < +125°C	TBD			
Input Capacitance	C_{INDM}	Differential mode		0.4		pF
	C_{INCM}	Common mode		3.6		pF
Input Resistance	R_{DIFF}	Differential mode		TBD		MΩ
	R_{CM}	Common mode		TBD		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	50	30		mV
		–40°C < T_A < +125°C	TBD			mV
		I_{SOURCE} = 15mA	700	500		mV
		–40°C < T_A < +125°C	TBD			mV
Output Voltage Low	V_{OL}	I_{SINK} = 1mA		45	65	mV
		–40°C < T_A < +125°C			TBD	mV
		I_{SINK} = 15mA		315	450	mV
		–40°C < T_A < +125°C			TBD	mV
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		TBD		mA
Short-Circuit Current	I_{SC}			55		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		TBD		Ω
		A_V = +10		TBD		Ω
		A_V = +100		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V	87	103		dB
		–40°C < T_A < +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}			665	700	µA
		–40°C < T_A < +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = ±12.5 V, R_L = 2 KΩ, C_L = 100 pF, Av = +1		20		V/µs
Gain Bandwidth Product	GBP	A_V = +100				MHz
Unity Gain Crossover	UGC	A_V = +1		7.5		MHz
-3dB Bandwidth	-3dB	A_V = +1				MHz

Phase Margin	Φ_M		TBD		Degrees
Settling Time to 0.1%	t_s	V_{IN} =10 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1	TBD		µs
Settling Time to 0.01%	t_s	V_{IN} =10 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1	TBD		µs
EMI Rejection	EMIRR				
f=1000MHz			TBD		dB
f=2400MHz			TBD		dB
NOISE PERFORMANCE					
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz	1		µV p-p
Voltage Noise Density	e_N	f = 10 Hz	TBD		nV/√Hz
		f = 100 Hz	TBD		nV/√Hz
		f = 1 kHz	12		nV/√Hz
		f = 10 kHz	12		nV/√Hz
Current Noise	i_N p-p	f = 0.1 Hz to 10 Hz	TBD		fA p-p
Current Noise Density	i_N	f = 1 kHz	TBD		fA/√Hz
Total Harmonic Distortion + Noise	THD+N	G= +1, f = 10Hz to 20kHz, V_{IN} = TBD V_{RMS} @ 1 kHz			
BW = 80 kHz			TBD		%
BW = 500 kHz			TBD		%
MATCHING SPECIFICATIONS					
Initial Offset Voltage			TBD	TBD	V
Maximum Offset Voltage over Temp			TBD		V
Offset Voltage Temperature Drift			TBD		µV/°C
Input Bias Current			TBD	TBD	pA
CROSSTALK (Dual Version Only)	C_S	f = 1 kHz	TBD		dB
		f = 100 kHz	TBD		dB

ELECTRICAL CHARACTERISTICS V_{SY} = ±5 V

V_{SY} = ±5 V, V_{CM} = V_{OUT} = 0 V, TA = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.04	±0.8	mV
		-40°C < T_A < +125°C			TBD	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C < T_A < +125°C		2	10	µV/°C
Input Bias Current	I_B			2	±10	pA
		-40°C < T_A < +125°C	–TBD		+TBD	pA
		V_{CM} = V-		-5		pA
Input Offset Current	I_{OS}			TBD	±10	pA
		-40°C < T_A < +125°C	–TBD		+TBD	pA
Input Voltage Range	IVR		V- - 0.2		V+ - 1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V- to V+ - 3 V	75	91		dB
		–40°C < T_A < +125°C	TBD			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_{OUT} = –4.5 V to +4.5 V	113	118		dB
		–40°C < T_A < +125°C	TBD			
		R_L = 1 kΩ, V_{OUT} = –4.4 V to +4.4 V	100	105		dB
		–40°C < T_A < +125°C	TBD			
Input Capacitance	C_{INDM}	Differential mode		0.4		pF
	C_{INCM}	Common mode		3.6		pF
Input Resistance	R_{DIFF}	Differential mode		TBD		MΩ
	R_{CM}	Common mode		TBD		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	50	30		mV
		–40°C < T_A < +125°C	TBD			mV
		I_{SOURCE} = 15mA	700	490		mV
		–40°C < T_A < +125°C	TBD			mV
Output Voltage Low	V_{OL}	I_{SINK} = 1mA		45	65	mV
		–40°C < T_A < +125°C			TBD	mV
		I_{SINK} = 15mA		315	450	mV
		–40°C < T_A < +125°C			TBD	mV
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		TBD		mA
Short-Circuit Current	I_{SC}			55		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		TBD		Ω
		A_V = +10		TBD		Ω
		A_V = +100		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V	87	103		dB
		–40°C < T_A < +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}			610	675	µA
		–40°C < T_A < +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_O = ±3 V, R_L = 2 KΩ, C_L = 100 pF, A_V = +1		20		V/µs
Gain Bandwidth Product	GBP	A_V = +100				MHz
Unity Gain Crossover	UGC	A_V = +1		7.5		MHz
-3dB Bandwidth	-3dB	A_V = +1				MHz
Phase Margin	Φ_M			TBD		Degrees

Settling Time to 0.1%	t_S	V_{IN} = 8 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1	TBD		µs
Settling Time to 0.01%	t_S	V_{IN} = 8 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1	TBD		µs
EMI Rejection	EMIRR				
f=1000MHz			TBD		dB
f=2400MHz			TBD		dB
NOISE PERFORMANCE					
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz	1		µV p-p
Voltage Noise Density	e_N	f = 10 Hz	TBD		nV/√Hz
		f = 100 Hz	TBD		nV/√Hz
		f = 1 kHz	12		nV/√Hz
		f = 10 kHz	12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz	TBD		pA/√Hz
Total Harmonic Distortion + Noise	THD+N	G= +1, f = 10Hz to 20kHz, V_{IN} = TBD V_{RMS} @ 1 kHz			
BW = 80 kHz			TBD		%
BW = 500 kHz			TBD		%
MATCHING SPECIFICATIONS					
Initial Offset Voltage			TBD	TBD	V
Maximum Offset Voltage over Temp			TBD		V
Offset Voltage Temperature Drift			TBD		µV/°C
Input Bias Current			TBD	TBD	pA
CROSSTALK (Dual Version Only)	C_S	f = 1 kHz	TBD		dB
		f = 100 kHz	TBD		dB

ELECTRICAL CHARACTERISTICS V_{SY} = 5 V

V_{SY} = 5 V, V_{CM} = 0 V, V_{OUT} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.4	±0.8	mV
		-40°C < T_A < +125°C			TBD	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C < T_A < +125°C		2	10	µV/°C
Input Bias Current	I_B			2	±10	pA
		-40°C < T_A < +125°C	–TBD		+TBD	pA
Input Offset Current	I_{OS}			TBD	±10	pA
		-40°C < T_A < +125°C	–TBD		+TBD	pA
Input Voltage Range	IVR		V- - 0.2		V+ - 1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V- to V+ - 3 V	70	87		dB
		–40°C < T_A < +125°C	TBD			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ to V-, V_{OUT} = 0.2 V to +4.6 V	110	115		dB
		–40°C < T_A < +125°C	TBD			
		R_L = 1 kΩ to V-, V_{OUT} = 0.2 V to +4.6 V	96	104		dB
		–40°C < T_A < +125°C	TBD			
Input Capacitance	C_{INDM}	Differential mode		0.4		pF
	C_{INCM}	Common mode		3.6		pF
Input Resistance	R_{DIFF}	Differential mode		TBD		MΩ
	R_{CM}	Common mode		TBD		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	50	30		mV
		–40°C < T_A < +125°C	TBD			mV
		I_{SOURCE} = 15mA	700	500		mV
		–40°C < T_A < +125°C	TBD			mV
Output Voltage Low	V_{OL}	I_{SINK} = 1mA		45	65	mV
		–40°C < T_A < +125°C			TBD	mV
		I_{SINK} = 15mA		310	450	mV
		–40°C < T_A < +125°C			TBD	mV
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		TBD		mA
Short-Circuit Current	I_{SC}			55		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		TBD		Ω
		A_V = +10		TBD		Ω
		A_V = +100		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 15 V	80	95		dB
		–40°C < T_A < +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}			600	650	µA
		–40°C < T_A < +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_O = 0.5 V to 3.5 V, R_L = 2 KΩ, C_L = 100 pF, A_V = +1		20		V/µs
Gain Bandwidth Product	GBP	A_V = +100				MHz
Unity Gain Crossover	UGC	A_V = +1		7.5		MHz
-3dB Bandwidth	-3dB	A_V = +1				MHz
Phase Margin	Φ_M			TBD		Degrees
Settling Time to 0.1%	t_s	V_{IN} = 4 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = –1		TBD		µs

Settling Time to 0.01%	t_s	V_{IN} = 4 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1	TBD		µs
EMI Rejection	EMIRR				
f=1000MHz			TBD		dB
f=2400MHz			TBD		dB
NOISE PERFORMANCE					
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz	1		µV p-p
Voltage Noise Density	e_N	f = 10 Hz	TBD		nV/√Hz
		f = 100 Hz	TBD		nV/√Hz
		f = 1 kHz	12		nV/√Hz
		f = 10 kHz	12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz	TBD		pA/√Hz
Total Harmonic Distortion + Noise	THD+N	G= +1, f = 10Hz to 20kHz, V_{IN} = TBD V_{RMS} @ 1 kHz			
BW = 80 kHz			TBD		%
BW = 500 kHz			TBD		%
MATCHING SPECIFICATIONS					
Initial Offset Voltage			TBD	TBD	V
Maximum Offset Voltage over Temp			TBD		V
Offset Voltage Temperature Drift			TBD		µV/°C
Input Bias Current			TBD	TBD	pA
CROSSTALK (Dual Version Only)	C_S	f = 1 kHz	TBD		dB
		f = 100 kHz	TBD		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	(V-) -0.3 V to (V+) +0.2V
Differential Input Voltage	TBD V
Storage Temperature Range	
R, RM, RJ, and RU Packages	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	
R, RM, RJ, and RU Packages	−65 °C to +150 °C
Lead Temperature, Soldering (10 sec)	300 °C
ESD Rating (HBM)	TBD

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance[1]

Package Type	θ_{JA}	Unit
8-lead SOIC		
1 layer JEDEC Board	196	°C/W
2 layer JEDEC Board	111	°C/W
8-lead MSOP		
1 layer JEDEC Board	TBD	°C/W
2 layer JEDEC Board	TBD	°C/W

[1] Thermal impedance simulated values are based on JEDEC thermal test board. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PR13502-0-8/15(PrA)